Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

Claim 1 (Currently amended): A semiconductor package which is positioned on a first substrate comprising:

a second substrate having a first surface and a second surface, wherein the second surface of the second substrate has a rectangular shape;

a chip positioned on the first surface of the second substrate;

a plurality of first bonding balls positioned on the second surface of the second substrate and arranged in a single row along a first direction for connecting the second substrate to the first substrate, wherein the first direction is parallel to a long side of the second surface; and

at least a rectangular-shaped dummy bonding bar positioned on the second surface of the second substrate for connecting the second substrate to the first substrate and preventing the semiconductor package from inclining to one side, wherein the dummy bonding bar and the first bonding balls are arranged in the single~~same~~ row.

Claim 2 (cancelled)

Claim 3 (original): The semiconductor package of claim 2 wherein the longest side of the dummy bonding bar is approximately perpendicular to the long side of the second surface for preventing the semiconductor package from inclining.

Claim 4 (original): The semiconductor package of claim 3 wherein a length of a short side of the second surface is less than 1000 μm.

Claim 5 (original): The semiconductor package of claim 1 wherein the dummy bonding

bar has a planar third surface connected to the first substrate for preventing the semiconductor package from inclining.

Claim 6 (original): The semiconductor package of claim 1 further comprising a plurality of first bonding pads, each of which being positioned between the second surface and each of the first bonding balls, and at least a dummy bonding pad positioned between the second surface and the dummy bonding bar.

Claim 7 (original): The semiconductor package of claim 6 further comprising a plurality of second bonding pads positioned on the second surface and a plurality of second bonding balls respectively positioned on the second bonding pads, the second bonding balls being interlaced with the first bonding balls.

Claim 8 (original): The semiconductor package of claim 7 wherein a height of the dummy bonding bar is the same as a height of each of the first bonding balls and the second bonding balls.

Claim 9 (previously presented): The semiconductor package of claim 7 wherein the first bonding balls, the second bonding balls and the dummy bonding bar respectively comprise a tin (Sn) based metal containing lead (Pb), and a melting point of the tin based metal is between 180℃ and 235℃.

Claim 10 (previously presented): The semiconductor package of claim 9 wherein the first bonding pads, the second bonding pads and the dummy bonding pad respectively comprise a tin based metal, which contains no lead and has a melting point between 180 ℃ and 235℃.

Claim 11 (original): The semiconductor package of claim 1 wherein the first substrate

comprises a build-up printed circuit board, a co-fired ceramic substrate, a thin-film deposited substrate, or a glass substrate.

Claim 12 (original): The semiconductor package of claim 1 wherein the chip is an image sensor chip.

Claim 13-25 (cancelled)

Claim 26 (new): A semiconductor package which is positioned on a first substrate comprising:

a second substrate having a first surface and a second surface;

a chip positioned on the first surface of the second substrate;

a plurality of first bonding balls positioned on the second surface of the second substrate and arranged in a single row along a first direction for connecting the second substrate to the first substrate; and

at least a dummy bonding bar positioned on the second surface of the second substrate and arranged in the single row with the first bonding balls for connecting the second substrate to the first substrate and preventing the semiconductor package with the single row of the first bonding balls and the dummy bonding bar from inclining to one side.

Claim 27 (new): The semiconductor package of claim 26 wherein the second surface has a rectangular shape, and the first direction is parallel to a long side of the second surface.

Claim 28 (new): The semiconductor package of claim 27 wherein the longest side of the dummy bonding bar is approximately perpendicular to the long side of the second surface for preventing the semiconductor package from inclining.

Claim 29 (new): The semiconductor package of claim 28 wherein a length of a short side of the second surface is less than 1000 μm.

Claim 30 (new): The semiconductor package of claim 26 wherein the dummy bonding bar has a planar third surface connected to the first substrate for preventing the semiconductor package from inclining.

Claim 31 (new): The semiconductor package of claim 26 further comprising a plurality of first bonding pads, each of which being positioned between the second surface and each of the first bonding balls, and at least a dummy bonding pad positioned between the second surface and the dummy bonding bar.

Claim 32 (new): The semiconductor package of claim 31 further comprising a plurality of second bonding pads positioned on the second surface and a plurality of second bonding balls respectively positioned on the second bonding pads, the second bonding balls being interlaced with the first bonding balls.

Claim 33 (new): The semiconductor package of claim 32 wherein a height of the dummy bonding bar is the same as a height of each of the first bonding balls and the second bonding balls.

Claim 34 (new): The semiconductor package of claim 32 wherein the first bonding balls, the second bonding balls and the dummy bonding bar respectively comprise a tin (Sn) based metal containing lead (Pb), and a melting point of the tin based metal is between 180℃ and 235℃.

Claim 35 (new): The semiconductor package of claim 34 wherein the first bonding pads, the second bonding pads and the dummy bonding pad respectively comprise a tin based

metal, which contains no lead and has a melting point between 180℃ and 235℃.

Claim 36 (new): The semiconductor package of claim 26 wherein the first substrate comprises a build-up printed circuit board, a co-fired ceramic substrate, a thin-film deposited substrate, or a glass substrate.

Claim 37 (new): The semiconductor package of claim 26 wherein the chip is an image sensor chip.